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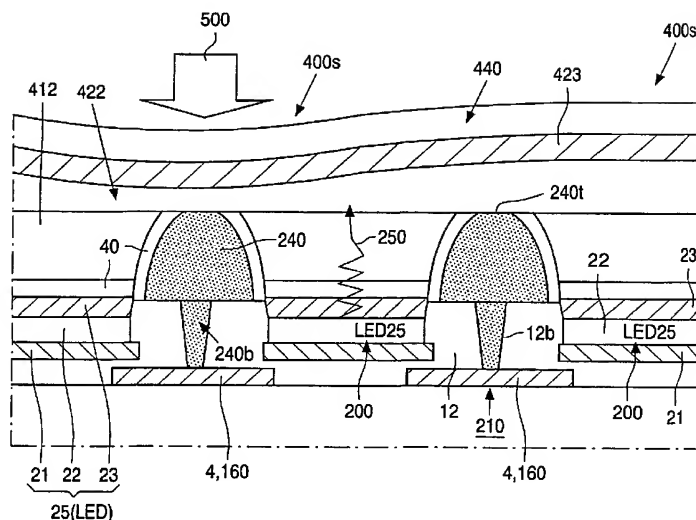
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(54) Title: ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICES, AND THEIR MANUFACTURE



(57) Abstract: Physical barriers (210) are present between neighbouring pixels (200) on a circuit substrate (100) of an active-matrix electroluminescent display device, particularly with LEDs (25) of organic semiconductor materials. The invention forms these barriers (210) with metal or other electrically-conductive material (240) that serves as an interconnection between a first circuit element (21, 4, 5, 6, 140, 150, 160, T1, T2, Tm, Tg, Ch) of the circuit substrate and a second circuit element (400, 400s, 23), for example, a sensor (400s) of a sensor array supported over the pixel array. The conductive barrier material (240) is insulated (40) at the sides of the barriers adjacent to the LEDs and has an un-insulated top connection area (240t) at which the second circuit element is connected to the conductive barrier material (240).



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## DESCRIPTION

**ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICES, AND  
THEIR MANUFACTURE.**

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This invention relates to active-matrix electroluminescent display devices, particularly but not exclusively using light-emitting diodes of semiconducting conjugated polymer or other organic semiconductor materials. The invention also relates to methods of manufacturing such devices.

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Such active-matrix electroluminescent display devices are known, comprising an array of pixels present on a circuit substrate, wherein each pixel comprises an electroluminescent element, typically of organic semiconductor material. The electroluminescent elements are connected to circuitry in the substrate, for example drive circuitry that includes supply lines and matrix addressing circuitry that includes addressing (row) and signal (column) lines. These lines are generally formed by thin-film conductor layers in the substrate. The circuit substrate also includes addressing and drive elements (typically thin-film transistors, hereafter termed "TFT"s) for each pixel.

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In many such arrays, physical barriers of insulating material are present between neighbouring pixels in at least one direction of the array. Examples of such barriers are given in published United Kingdom patent application GB-A-2 347 017, published PCT patent application WO-A1-99/43031, published European patent applications EP-A-0 895 219, EP-A-1 096 568, and EP-A-1 102 317, the whole contents of which are hereby incorporated herein as reference material.

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Such barriers are sometimes termed "walls", "partitions", "banks", "ribs", "separators", or "dams", for example. As can be seen from the cited references, they may serve several functions. They may be used in manufacture to define electroluminescent layers and/or electrode layers of the individual pixels and/or of columns of pixels. Thus, for example, the barriers prevent pixel overflow of conjugate polymer materials that may be ink-jet

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printed for red, green and blue pixels of a colour display or spin-coated for a monochrome display. The barriers in the manufactured device can provide a well-defined optical separation of pixels. They may also carry or comprise conductive material (such as upper electrode material of the electroluminescent element), as auxiliary wiring for reducing the resistance of (and hence the voltage drops across) the common upper electrode of the electroluminescent elements.

It is an aim of the present invention to enhance the capabilities and/or performance of active-matrix electroluminescent display devices, in a manner that is compatible with the basic device structure, its layout and its electronics.

According to one aspect of the present invention, there is provided an active-matrix electroluminescent display device having the features set out in Claim 1.

In accordance with the invention, the physical barriers between pixels are used to provide interconnections between a first circuit element of the circuit substrate and a second circuit element that is connected at the top of the barrier. Thus, these pixel barriers are partly (possibly even predominantly) of electrically-conductive material (typically metal) which provides the interconnection, while also being insulated at least at the sides of the barriers adjacent to the electroluminescent elements.

Much versatility is possible in accordance with the invention. Various layout features can be adopted for the pixel barriers, depending on the circuit elements being interconnected. Thus, the conductive barrier material may provide interconnections that are localised to, for example, individual pixels or groups of pixels, or interconnections that may be located outside the pixel array. Thus, each un-insulated top connection area may itself be localised as part of a connection pattern along the top of the barriers, and/or the interconnecting conductive barrier material may be localised in, for example, separately insulated lengths of the barriers.

The first and second circuit elements may take a variety of forms, depending on the particular improvement or enhancement or adaptation being

made. Typically, the first circuit element of the circuit substrate may be one or more thin-film elements of the group comprising: a conductor layer; an electrode connection; a supply line; an addressing line; a signal line; a thin-film transistor; a thin-film capacitor. The second circuit element may be another  
5 such thin-film element in the circuit substrate and/or, for example, an electrode connection of the electroluminescent element of a respective pixel or an added component such as a sensor.

The last possibility permits various forms of sensor array to be integrated together with the array of pixels. The sensor array may be  
10 integrated within the circuit substrate. However, the sensor array may be supported on top of the barriers and over the pixel array. This provides a compact layout and is particularly suitable for direct pen input and/or finger-print sensing. The sensor array may even share matrix addressing circuitry of the pixel array in the circuit substrate. This simplifies the integration  
15 of the sensor array with the pixel array. Sharing may be achieved in a manner similar to that disclosed in, for example, United States patents US-A-5,386,543 and US-A-5,838,308 (Philips refs: PHB33816 and PHB33715). The whole contents of US-A-5,386,543 and US-A-5,838,308 are hereby incorporated herein as reference material.

20 As well as using the barriers to provide interconnections in accordance with the present invention, the barriers (or at least other separately insulated lengths of the barriers) may serve different functions. They may be used to form, for example, a component such as a capacitor or inductor or transformer and/or to back-up or replace thin-film conductor lines of the circuit substrate.  
25 These back-up or replacement lines may be, for example an address line, a signal line or a supply line.

According to another aspect of the present invention, there are also provided advantageous methods of manufacturing such an active-matrix electroluminescent display device.

30 Various advantageous features and feature-combinations in accordance with the present invention are set out in the appended Claims.

These and others are illustrated in embodiments of the invention that are now described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram for four pixel areas of an active-matrix electroluminescent display device which can be provided with interconnections in accordance with the invention;

Figure 2 is a cross-sectional view of part of the pixel array and circuit substrate of one embodiment of such a device, showing one example of a conductive barrier construction for forming interconnections to a TFT source or drain line in accordance with the invention;

Figure 3 is a cross-sectional view of part of the pixel array and circuit substrate of a similar embodiment of such a device, showing another example of a conductive barrier construction for forming interconnections to a TFT gate line in accordance with the invention;

Figure 4 is a cross-sectional view of the interconnection part of such an embodiment as that of Figure 2 or Figure 3, showing an example of a modified conductive barrier construction that uses a metal coating for forming interconnections in accordance with the invention;

Figure 5 is a cross-sectional view of part of such a device such as that of Figure 2 or Figure 3, showing interconnections in accordance with the invention for a pressure sensor integrated with the electroluminescent device;

Figure 6 is a cross-sectional view of part of such a device such as that of Figure 2 or Figure 3, showing interconnections in accordance with the invention for a capacitance sensor integrated with the electroluminescent device;

Figure 7 is a cross-sectional view of part of such a device such as that of Figure 2 or Figure 3, showing interconnections in accordance with the invention for a direct input sensor integrated with the electroluminescent device;

Figure 8 is a cross-sectional view of part of such a device such as that of Figure 2 or Figure 3, showing interconnections in accordance with the invention between upper and lower electrodes of adjacent pixels or sub-pixels;

Figure 9 is a plan view of four pixel areas showing a specific example of layout features for a particular embodiment of a device in accordance with the invention, with side-by-side conductive barriers;

Figure 10 is a cross-sectional view through the side-by-side barriers of Figure 9, taken on the line X-X of Figure 9;

Figure 11 is a plan view of another example of layout features for a particular embodiment of a device in accordance with the invention, with transverse conductive barriers;

Figure 12 is a sectional view of a device part with yet another example of a conductive barrier construction for forming interconnections in accordance with the invention;

Figures 13 to 16 are sectional views of a device part such as that of Figure 2 or Figure 3 at stages in its manufacture with one particular embodiment in accordance with the invention; and

Figure 17 is a sectional view a device part at the insulation stage, illustrating a modification in the insulation of the conductive barrier interconnections that is also in accordance with the present invention.

It should be noted that all the Figures are diagrammatic. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in modified and different embodiments.

#### Embodiments of Figures 1 to 4

The active-matrix electroluminescent display device of each of the Figures 1 to 4 embodiments comprises an array of pixels 200 on a circuit substrate 100 with matrix addressing circuitry. Physical barriers 210 are present between at least some of the neighbouring pixels in at least one direction of the array. At least some of these barriers 210 are constructed with conductive barrier material 240 that is used as an interconnection in accordance with the present invention. Apart from this special construction and use of the barriers 210 in accordance with the present invention, the

display may be constructed using known device technologies and circuit technologies, for example as in the background references cited hereinbefore.

The matrix addressing circuitry comprises transverse sets of addressing (row) and signal (column) lines 150 and 160, respectively, as illustrated in Figure 1. An addressing element T2 (typically a thin-film transistor, hereafter termed "TFT") is incorporated at each interception of these lines 150 and 160. It should be understood that Figure 1 depicts, by way of example, one specific pixel circuit configuration. Other pixel circuit configurations are known for active matrix electroluminescent display devices. It should readily be understood that the present invention may be applied to the pixel barriers of such a device regardless of the specific pixel circuit configuration of the device.

Each pixel 200 comprises a current-driven electroluminescent element 25 (21,22,23), typically a light-emitting diode (LED) of organic semiconductor material. The LED 25 is connected in series with a drive element T1 (typically a TFT) between two voltage supply lines 140 and 230 of the array. These two supply lines are typically a power supply line 140 (with voltage Vdd) and a ground line 230 (also termed "return line"). Light emission from the LED 25 is controlled by the current flow through the LED 25, as altered by its respective drive TFT T1.

Each row of pixels is addressed in turn in a frame period by means of a selection signal that is applied to the relevant row conductor 150 (and hence to the gate of the addressing TFTs T2 of the pixels of that row). This signal turns on the addressing TFT T2, so loading the pixels of that row with respective data signals from the column conductors 160. These data signals are applied to the gate of the individual drive TFT T1 of the respective pixel. In order to hold the resulting conductive state of the drive TFT T1, this data signal is maintained on its gate by a holding capacitor Ch that is coupled between this gate and the drive line 140,240. Thus, the drive current through the LED 25 of each pixel 200 is controlled by the driving TFT T1 based on a drive signal applied during the preceding address period and stored as a voltage on the associated capacitor Ch. In the specific example of Figure 1, T1 is shown as a P-channel TFT, whereas T2 is shown as an N-channel TFT.

This circuitry can be constructed with known thin-film technology. The substrate 100 may have an insulating glass base 10 on which an insulating surface-buffer layer 11, for example, of silicon dioxide is deposited. The thin-film circuitry is built up on the layer 11 in known manner.

5        Figures 2 and 3 show TFT examples T<sub>m</sub> and T<sub>g</sub>, each comprising: an active semiconductor layer 1 (typically of polysilicon); a gate dielectric layer 2 (typically of silicon dioxide); a gate electrode 5 (typically of aluminium or polysilicon); and metal electrodes 3 and 4 (typically of aluminium) which contact doped source and drain regions of the semiconductor layer 1 through  
10        windows (vias) in the over-lying insulating layer(s) 2 and 8. Extensions of the electrodes 3, 4 and 5 may form, for example, interconnections between the elements T<sub>1</sub>, T<sub>2</sub>, Ch and LED 25, and/or at least part of the conductor lines 140, 150 and 160, depending on the circuit function provided by the particular TFT (for example, the drive element T<sub>1</sub> or the addressing element T<sub>2</sub> or  
15        another TFT of the circuit substrate). The holding capacitor Ch may be formed similarly, in known manner, as a thin-film structure inside the circuit substrate 100.

      The LED 25 typically comprises a light-emitting organic semiconductor material 22 between a lower electrode 21 and an upper electrode 23. In a  
20        preferred particular embodiment, semiconducting conjugated polymers may be used for the electroluminescent material 22. For a LED that emits its light 250 through the substrate 100, the lower electrode 21 may be an anode of indium tin oxide (ITO), and the upper electrode 23 may be a cathode comprising, for example, calcium and aluminium. Figures 2 and 3 illustrate a LED  
25        construction in which the lower electrode 21 is formed as a thin film in the circuit substrate 100. The subsequently-deposited organic semiconductor material 22 contacts this thin-film electrode layer 21 at a window 12a in a planar insulating layer 12 (for example of silicon nitride) that extends over the thin-film structure of the substrate 100.

30        As in known devices, the devices of Figures 1 to 4 in accordance with the present invention include physical barriers 210, between at least some of the neighbouring pixels in at least one direction of the array. These barriers

210 may also be termed "walls", "partitions", "banks", "ribs", "separators", or "dams", for example. Depending on the particular device embodiment and its manufacture, they may be used in known manner, for example:

- 5       • to separate and prevent overflow of a polymer solution between the respective areas of the individual pixels 200 and/or columns of pixels 200, during the provision of semiconducting polymer layers 22;
- 10       • to provide a self-patterning ability on the substrate surface in the definition of the semiconducting polymer or other electroluminescent layers 22 for the individual pixels 200 and/or for columns of pixels 200 (and possibly even a self-separation of individual electrodes for the pixels, for example an individual bottom layer of the upper electrodes 23);
- 15       • to act as a spacer for a mask over the substrate surface during the deposition of at least an organic semiconductor material 22 and/or electrode material;
- to form opaque barriers 210 for a well-defined optical separation of the pixels 200 in the array, when light 250 is emitted through the top (instead of, or as well as, the bottom substrate 100).

20       Whatever their specific use in these known ways, at least some insulated portions of the physical barriers 210 in embodiments of the present invention are constructed and used in a special manner. Thus, the pixel barriers 210 of Figures 2 to 4 comprise metal 240 (or other electrically-conductive material 240) that is insulated from the LEDs 25 and that provides an interconnection between a first circuit element of the circuit substrate 100 and a second circuit element of the device. These circuit elements are  
25       connected at un-insulated bottom and top connection areas 240b, 240t of the conductive barrier material 240.

30       The first and second circuit elements may take a variety of forms, depending on the particular improvement or enhancement or adaptation being made. Typically, the first circuit element of the circuit substrate 100 may be one or more thin-film elements of the group comprising: a conductor layer and/or an electrode connection 4, 5, 6; a supply line 140; an addressing line

150; a signal line 160; a thin-film transistor T1, T2, Tm, Tg; a thin-film capacitor Ch. The second circuit element may be another such thin-film element in the circuit substrate 100 and/or, for example, an electrode connection of the LED 25 of a respective pixel or an added component such as a sensor.

5        Figures 2 to 4 show the un-insulated top connection area 240t, but without any specific second circuit element (upper circuit element 400) connected thereto. Particular examples of a second circuit element are described below with reference to Figures 5 to 8. However, it should readily be understood that the present invention can be applied to the interconnection  
10 of a wide variety of upper circuit elements 400 to circuitry in the circuit substrate 100 by means of such pixel barriers 210 in accordance with the invention.

      In the embodiment of Figure 2, the first circuit element is an extension of the source and/or drain electrode of TFT Tm. It may form a signal (column)  
15 line 160, for example, of the substrate circuitry when Tm is T2, or a drive line 140 when Tm is T1. In the embodiment of Figure 3, the first circuit element is an extension of the gate electrode 5 of TFT Tg. It may form an addressing (row) line 150, for example, of the substrate circuitry when Tg is T2.

      Figures 2 and 3 show the bottom connection of the conductive barrier  
20 material 240 to the first circuit element 4,5 at connection windows 12b in the intermediate insulating layer 12. However, it should be understood that these windows 12b may often not be in the same plane as the TFT Tm, Tg. In particular, there is generally insufficient space between the source and drain electrodes 3 and 4 of TFT Tg to accommodate a window 12b. Thus, the  
25 window 12b is depicted in broken outline in Figure 3 to indicate its location outside the plane of the drawing paper.

      The pixel barriers 210 in the embodiments of Figures 2 to 4 are predominantly of electrically-conductive material 240, 240x, preferably metal for very low resistivity (for example aluminium or copper or nickel or silver).  
30 The barriers 210 of Figures 2 and 3 comprise a bulk or core of the conductive material that provides the interconnection 240 and that has an insulating coating 40 on its sides and on its top (except where the top connection area

240t is exposed). The barrier 210 of Figure 4 comprises a bulk or core of conductive material 240x that has an insulating coating 40x on its sides and on its top. The conductive material that provides the interconnection 240 in Figure 4 is a metal coating that extends on the insulating coating 40x. An  
5 insulating coating 40 extends on the sides and on the top of the metal coating 240, except where the top connection area 240t is exposed. This structure of Figure 4 is more versatile than that of Figures 2 and 3. It permits the metal core 240x to be used for another purpose, for example, to back-up or even replace the lines 140, 150 or 160, so reducing their line resistance. The  
10 interconnection metal coating 240 may even be localised to specific locations along the barrier 210 where these interconnections are required, for example at individual pixels or sub-pixels.

#### Embodiments of Figures 5 to 7 with Sensor Arrays

15 In each of the embodiments of Figures 5 to 7, an array of sensors 400s is integrated together with the array of pixels 200. The sensors 400s provide the second circuit elements 400 that are connected by the conductive barrier material 240 to the first circuit element of the circuit substrate 100. A variety of sensor arrays may be integrated with the display in accordance with the  
20 invention. Thus, the sensing array may have, for example, a short-circuit touch input, or a pressure input, or a capacitance input, or a light-pen input.

For individual interconnections from a two-dimensional sensor array, the conductive barrier material 240 is generally split up into respective insulated lengths in the barriers 210, corresponding to the individual sensors 400s.

25 In this integrated sensor situation, the first circuit element may be, for example, a source/drain 4 or gate 5 of a TFT in the substrate 100. Preferably, the first circuit element is part of matrix addressing circuitry for both the array of pixels 200 and the array of sensors 200s. Thus, the first circuit element may be the source/drain line 4, 160 of TFT T2 for pixel addressing.

30 In each of the embodiments of Figures 5 to 7, the sensing capability is provided at the front of the display, through which the light 250 is emitted. The sensor array is supported on top of the barriers 210 and over the pixel array.

An insulating planarising layer 412 is present over the pixel array, with a thickness that extends to the top of the barriers 210 to support the sensor array over the pixel array. Although Figures 5 to 8 illustrate an interconnecting metal-core structure as in Figures 2 and 3, modifications are possible using, for example, an interconnecting metal-coating structure as in Figure 4.

The Figure 5 embodiment illustrates a pressure sensor structure comprising a compressible layer 422 of dielectric or highly resistive material. This compressible layer is stacked between a transparent upper electrode layer 423 of, for example, ITO and the underlying conductive barrier material 240 and insulating planarising layer 412. The upper electrode layer 423 is coated with a protective layer 440. When pressure 500 is applied to this stack, the spacing between the electrode layer 423 and the conductive barrier material changes causing either a measurable change in capacitance across the dielectric or a reduction in resistance across the highly resistive material. This is a most advantageous embodiment, in that the electrode layer 423 also provides ESD protection for the circuit inputs.

Figure 6 illustrates a capacitive sensor, for example a finger-print sensor. An array of electrode pads 421 of ITO or metal are connected at the top of the corresponding array of conductive barrier material 240 to form one plate of a respective capacitor having thereon a capacitor dielectric layer 430. The other plate of the capacitor is formed by a finger or other object to be sensed, when placed on the dielectric layer 430.

Figure 7 illustrates a direct input sensor having electrode pads 424 of ITO that are connected at the top of the corresponding array of conductive barrier material 240. The direct input may be a current or voltage input from, for example, a wired pen that touches the pads 424. Alternatively, the direct input may simply be a short-circuit by an (un-wired) conductive pen between neighbouring pads 424, for example between a pad 424 connected to a row conductor 150 and a pad 424 connected to a column conductor 160. Current flow resulting from such a short-circuit can be measured at the periphery of the display to determine which pixel was shorted.

### Embodiment of Figure 8 with Pixel or Sub-Pixel Interconnect

The second circuit element in the embodiment of Figure 8 is an upper electrode 23 of the LED 25, which is connected by the conductive barrier material 240 to a thin-film element of the circuit substrate 100. Such an interconnection permits the integration of circuitry to both electrodes 21 and 23 of the given LED 25.

However, in the particular embodiment depicted in Figure 8, the bottom connection of the conductive barrier material 240 is to a thin-film element that forms the lower electrode of a neighbouring LED 25. Such a construction can be adopted for a display each pixel of which comprises, for example, side-by-side sub-pixels with the barriers 210 there-between. In this case, the conductive barrier material 240 connects the upper electrode 23 of one sub-pixel 200b to the lower electrode 21 of an adjacent sub-pixel 200a.

### Layout Embodiments of Figures 9 and 10 and of Figure 11

A wide variety of layout configurations are possible for the interconnect barrier material 240 in devices in accordance with the invention. Advantageously, the interconnect barrier material 240 may be combined in a composite layout with other sections of barrier 210x between the pixels.

Figures 9 and 10 illustrate one composite layout in which the conductive barrier material 240x of the additional barrier sections 210x may back up or even replace the drive supply lines 140 of the substrate 100. The matrix thin-film circuit area is designated as 120 in Figure 9. In this particular example, the insulated lengths of the interconnect barrier material 240 extend parallel to the additional barrier lines 210x, 140.

Figure 11 illustrates another composite layout in which the additional barrier sections 210x (240x, 40x) are transverse to the interconnect barrier material 240. In this case, the conductive barrier material 240x of the additional barrier sections 210x may back up or even replace the lines 140 or 150 or 160 of the substrate 100. Alternatively, the conductive barrier material 240x of the additional barrier sections 210x may form transverse interconnects for a direct-input sensor array such as that of Figure 7.

### Modified Barrier Embodiment of Figure 12

In the embodiments of Figures 2 to 8 and Figure 10, barriers 210 and 210x are shown as being predominantly of conductive material 240 and 240x. Figure 12 shows a modified embodiment wherein the barrier 210 is predominantly of insulating material 244. In this case, vias 244b are etched or milled through the insulating material 244 to the circuit element 4, 5 in the circuit substrate 100. A metal coating 240 provides the conductive barrier material that extends on top of the insulating barrier 210 and in the vias 244b therethrough.

The metal coating 240 of the barrier 210 may be formed simultaneously with a main part 23a of the upper electrode 23 of the LED 25, in a self-aligned manner. Thus, a layer of metal may be deposited simultaneously for the metal coating 240 and electrode 23 which are separated by a shadow-masking effect of an overhang shape in the side of the barrier 210, as illustrated in Figure 12. This is one possible process embodiment for forming barrier interconnects 210, 240 in accordance with the present invention. Figures 14 to 17 illustrate other process embodiments for barrier interconnects 210, 240 that are predominantly of metal.

### Process Embodiment of Figures 13 to 16

Apart from constructing and using its barriers 210 with interconnection material 240, the active-matrix electroluminescent display of a device in accordance with the present invention may be constructed using known device technologies and circuit technologies, for example as in the cited background references.

Figures 13 to 16 illustrate novel process steps in a particular manufacturing embodiment. The thin-film circuit substrate 100 with its upper planar insulating layer 12 (for example, of silicon nitride) is manufactured in known manner. Connection windows (such as vias 12a, 12b, 12x etc.) are opened in the layer 12 in known manner, for example by photolithographic masking and etching. However, in order to manufacture a device in

accordance with the present invention, the pattern of these vias include the vias 12b, 12x that expose elements 4, 5, 150, etc. for bottom connection with the conductive barrier material 240, 240x. The resulting structure is illustrated in Figure 13. This stage is common regardless of whether the barriers 210 are  
5 predominantly of conductive material as in Figures 2 to 8 and Figure 10 or predominantly of insulating material as in Figure 12.

The formation of barriers 210 predominantly of insulating material has been described above with reference to Figure 12. Suitable process steps for barriers 210 predominantly of conductive material (as in Figures 2 to 8 and  
10 Figure 10) will now be described with reference to Figures 14 to 16.

In this case, electrically-conductive material for the barriers 210 is deposited on the insulating layer 12 at least in its vias 12a, 12b, 12x etc. The desired lengths and layout pattern for the barriers 210 is obtained using known masking techniques. Figure 14 illustrates an embodiment in which at least the  
15 bulk 240 of the conductive barrier material (for example, copper or nickel or silver) is deposited by plating. In this case, a thin seed layer 240a of, for example, copper or nickel or silver is first deposited over the insulating layer 12 and its vias 12a, 12b, 12x etc, the barrier layout pattern is defined with a photolithographic mask, and then the bulk 240 of the conductive barrier  
20 material is plated to the desired thickness. The resulting structure is illustrated in Figure 14.

Then, using CVD (chemical vapour deposition), insulating material (for example silicon dioxide or silicon nitride) is deposited for the insulating coating 40. The deposited material is left on the sides and top of the conductive  
25 barrier material by patterning using known photolithographic masking and etching techniques. Thereafter the manufacture is continued in known manner to form the LEDs 25. Thus, for example, conjugate polymer materials 22 may be ink-jet printed or spin-coated for the pixels 200. The barriers 240,40 with their insulating coating 40 can be used in known manner to prevent polymer  
30 overflow from the pixel areas in between the physical barriers 240,40. The upper electrode material 23 is deposited on the layer 22. The resulting structure is illustrated in Figure 15.

Thereafter, in the case of the sensors of Figures 5 to 7, a layer of planarising material 412' is put down over the LEDs 25. This layer 412' may be etched back to expose the insulating coating 40 at the top of the barriers 210. This exposed top part of the insulating coating 40 may then be etched  
5 away to form the un-insulated top connection area 240t of the barrier 210, as illustrated in Figure 16. The sensor structure is then provided on top of this connection area 240t and planarising layer 412.

#### Modified Process Embodiment of Figure 17

10 This embodiment uses an anodisation treatment (instead of deposition) to provide the insulating coating 40 at least at the sides of the barriers 210 adjacent to the pixel areas. Typically, the conductive barrier material 240 may comprise aluminium. The desired lengths and layout pattern of the deposited aluminium can be defined using known photolithographic masking and etching  
15 techniques. Figure 17 shows the photolithically-defined etchant-mask 44 retained on the top of the aluminium barrier pattern 240.

Then, an anodic insulating coating of aluminium oxide is formed on at least the sides of the aluminium barrier material 240 using known anodisation techniques. Thus, no extra mask is needed to define the layout for this coating  
20 40.

As illustrated in Figure 17, the mask 44 can be retained during this anodisation, in areas where it is desired to protect and form the un-insulated top connection area 240t. In these areas, the anodic coating is formed at only the sides of the aluminium barrier pattern 240. The mask 44 may be removed  
25 before this anodisation, from areas where the anodic coating is required at both the sides and top of the aluminium barrier pattern 240. Alternatively, the mask 44 of an insulating polymer or, for example, silicon dioxide or nitride may be retained in these areas where insulation is desired over the top of the barrier 210(240,40) in the manufactured device.

30 In the embodiments described so far, the conductive barrier material 240 is a thick opaque metal, for example, aluminium, copper, nickel or silver.

However, other conductive materials 240 may be used, for example a metal silicide or (less advantageously) a degenerately-doped polysilicon both of which may be surface-oxidised to form the insulating coating 40. If transparent barriers 210 are required, then ITO may be used for the conductive barrier material 240.

5 Furthermore, it should be noted that line resistance can be significantly reduced by using conductive barrier material 240,240x to replace or to back up a conductor line (for example, 140, 150 or 160) of the circuit substrate 10. Thus, along a given line, the conductive barrier material 240 can have a cross-sectional area that is at least twice (possibly even an order of magnitude) larger than that of a typical conductor layer in the circuit substrate 100 (for  
10 example, a source/drain line 4,6 (140,160) of TFT T<sub>m</sub>, or a gate line 5 (150) of TFT T<sub>g</sub>). Typically, the conductive barrier material 240 may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this TFT conductor layer in the circuit substrate 100. In a  
15 specific example Z may be between 2µm and 5µm as compared with 0.5µm or less for z. Typically, the conductive barrier material 240 may have a line width Y that is the same width (or even at least twice as large) as the line width y of the TFT conductor layer. In a specific example Y may be 20µm as compared with 10µm for y.

20 From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the art (for example in the cited background references) and which may be used instead of or in addition to features already described herein.

25 Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as  
30 presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

The Applicants hereby give notice that new Claims may be formulated to any such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

## CLAIMS:

1. An active-matrix electroluminescent display device comprising: a circuit substrate on which an array of pixels is present with physical barriers  
5 between at least some of the neighbouring pixels in at least one direction of the array; each pixel comprising an electroluminescent element; the circuit substrate comprising circuitry to which the electroluminescent elements are connected; the physical barriers comprising conductive material that serves as an interconnection between a first circuit element of the circuit substrate and a  
10 second circuit element of the device; which conductive barrier material is insulated at least at the sides of the barriers adjacent to the electroluminescent elements and has top and bottom connection areas that are un-insulated where the first and second circuit elements are connected to the conductive barrier material.

15

2. A device according to Claim 1, wherein the first circuit element of the circuit substrate is at least one thin-film element of a group comprising: a conductor layer; an electrode connection; a supply line; an addressing line; a signal line; a thin-film transistor; a thin-film capacitor.

20

3. A device according to Claim 1, wherein the second circuit element is an upper electrode of the electroluminescent element, and the first circuit element is at least one thin-film element of the circuit substrate.

25

4. A device according to Claim 3, wherein each pixel comprises side-by-side sub-pixels with the barriers there-between and with the conductive barrier material connecting the upper electrode of one sub-pixel to the lower electrode of an adjacent sub-pixel, which lower and upper electrodes form the first and second circuit elements.

30

5. A device according to Claim 1 or Claim 2, wherein an array of sensors is integrated together with the array of pixels, and the sensors provide

the second circuit elements that are connected by the conductive barrier material to the first circuit element of the circuit substrate.

6. A device according to any one of the preceding Claims, wherein  
5 an array of sensors is integrated together with the array of pixels, the circuit substrate comprises matrix addressing circuitry for both the array of pixels and the array of sensors, and the conductive barrier material connects sensors of the array to the matrix addressing circuitry.

10 7. A device according to Claim 5 or Claim 6, wherein the sensor array is supported on top of the barriers and over the pixel array.

8. A device according to Claim 7, wherein a planarising layer is  
15 present over the pixel array with a thickness that extends to the top of the barriers to support the sensor array over the pixel array.

9. A device according to any one of the preceding Claims, wherein  
insulated lengths of the barriers are predominantly of the conductive barrier material (and preferably comprising metal).

20

10. A device according to any one of the preceding Claims, wherein  
the barrier comprises a metal core which provides the conductive barrier material that is connected with the first circuit element and that has an insulating coating on at least its sides.

25

11. A device according to any one of Claims 1 to 9, wherein the  
barrier comprises a metal coating which provides the conductive barrier material that is connected with the first circuit element and that has an insulating coating on at least its sides.

30

12. A device according to any one of Claims 1 to 8, wherein the  
physical barrier is predominantly of insulating material through which vias

extend for connection with the circuit element in the circuit substrate, and wherein a metal coating that provides the conductive barrier material extends on top of the physical barrier and in the vias through the physical barrier.

5           13.    A device according to any one of the preceding Claims, wherein the electroluminescent element is a current-driven light-emitting diode of organic semiconductor material.

10           14.    A device according to any one of the preceding Claims, wherein, under the conductive barrier material, connection windows are present in an intermediate insulating layer on the circuit substrate to permit connection to the first circuit element.

15           15.    A method of manufacturing an active-matrix electroluminescent display device according to any one of the preceding Claims, including the steps of:

20           (a)    forming the physical barriers with electrically-conductive material that is deposited on electrode connections to the first circuit element of the circuit substrate and with insulation at least at the sides of the physical barriers adjacent to the pixel areas, the physical barriers having an un-insulated top connection area to the conductive barrier material at the top of the barriers;

          (b)    providing at least part of the electroluminescent elements in the pixel areas in between the physical barriers; and

25           (c)    providing the second circuit element in connection with the conductive barrier material at the un-insulated top connection area of the barriers.

30           16.    A method according to Claim 15, wherein the insulation comprises an insulating coating that is deposited on at least the sides and top of the conductive barrier material and that is subsequently etched from the top connection area.

17. A method according to Claim 15, wherein the conductive barrier material comprises aluminium, and the insulation comprises an insulating coating that is formed on the sides of the aluminium barrier material by anodisation, while masking the top connection area against anodisation.

5

18. A method according to Claim 15, wherein the step (a) involves forming the physical barrier predominantly of insulating material through which vias are formed for connection with the circuit element at the connection windows on the circuit substrate, and wherein the electrically-conductive material is deposited as a conductive coating on top of the physical barrier and in the vias through the physical barrier.

10

19. A method according to Claim 18, wherein the conductive coating for the physical barrier and an upper electrode of the electroluminescent element are deposited simultaneously and are separated by a shadow-masking effect of an overhang shape in the side of the physical barrier.

15

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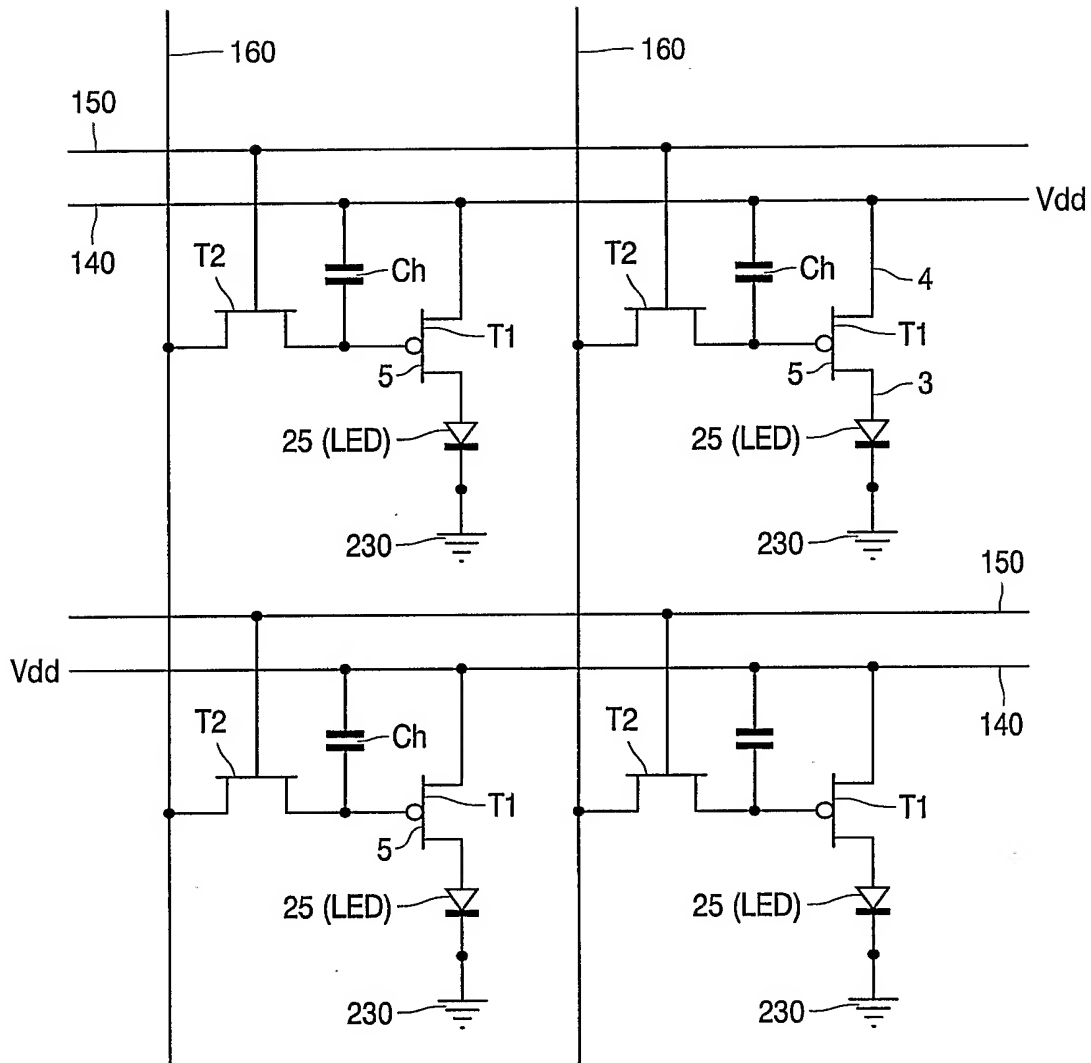


FIG. 1

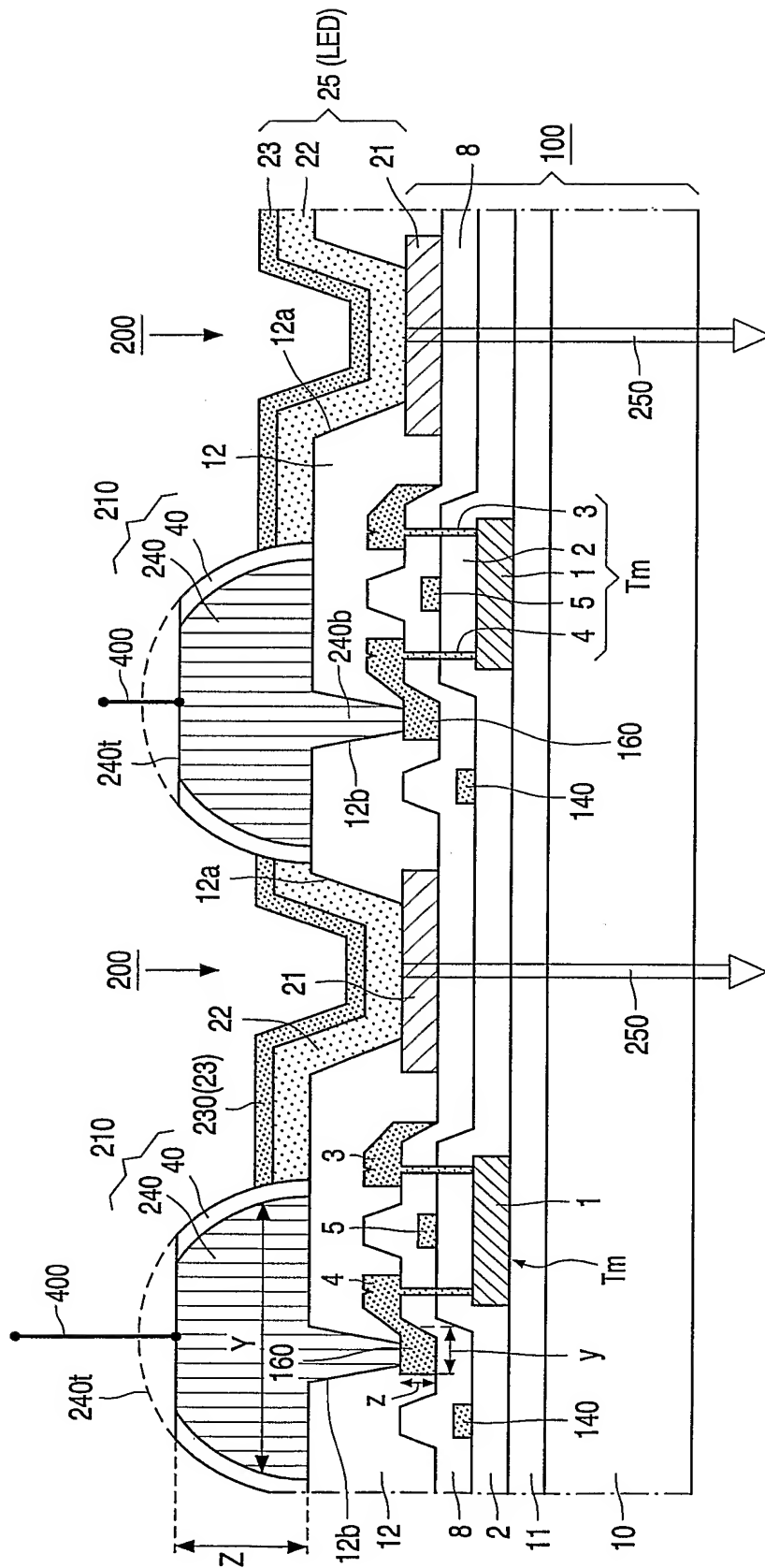


FIG. 2

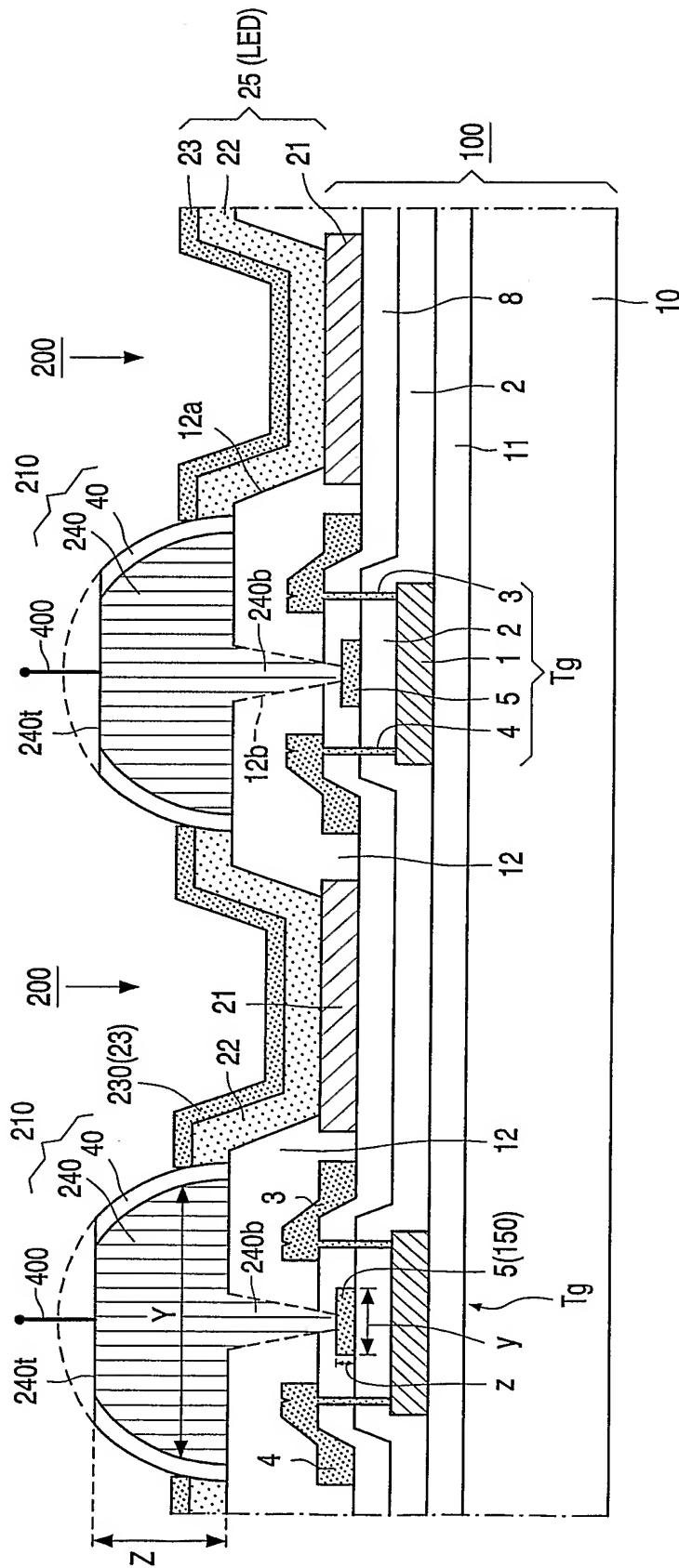


FIG. 3

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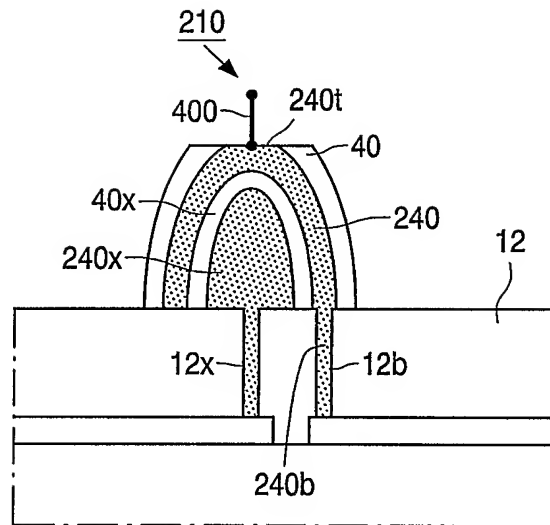


FIG. 4

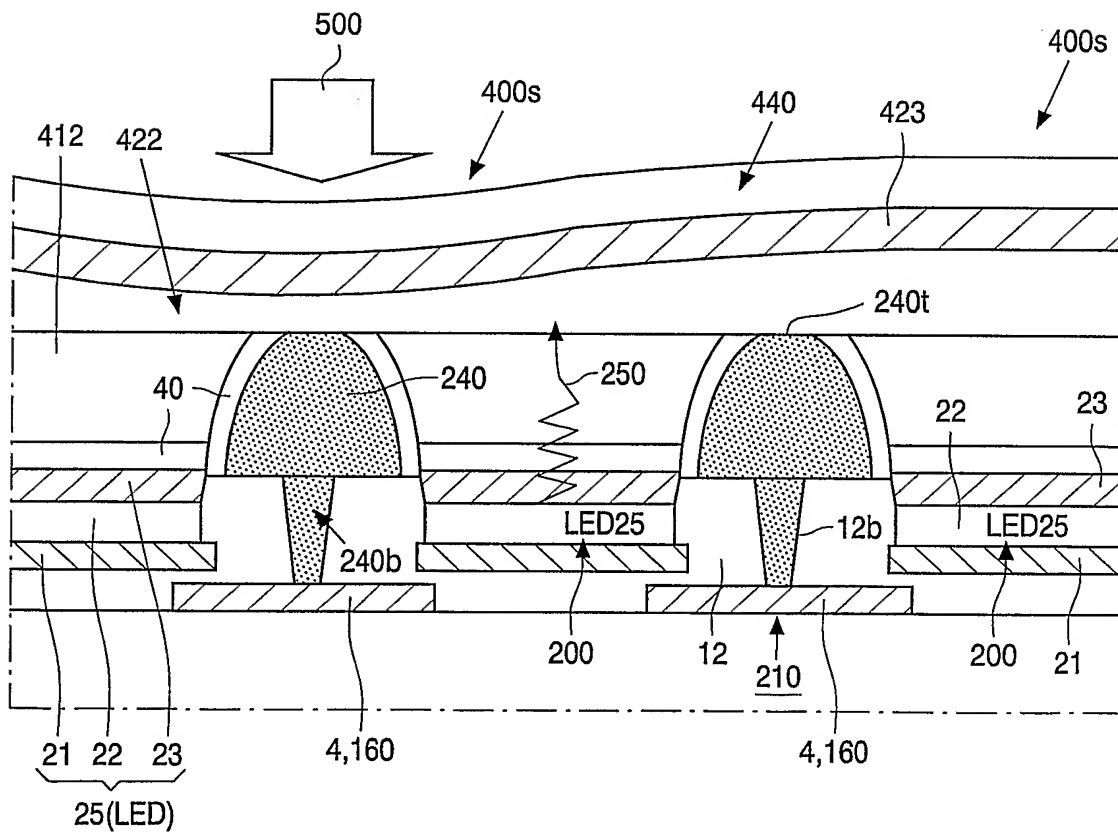


FIG. 5

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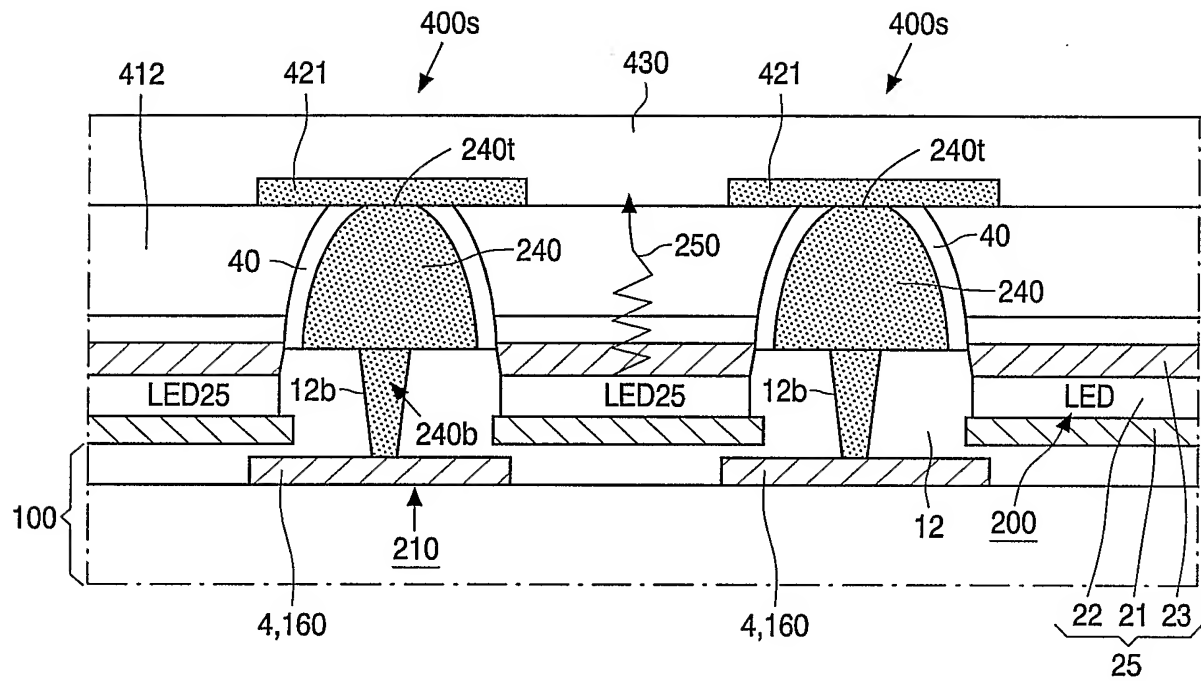


FIG. 6

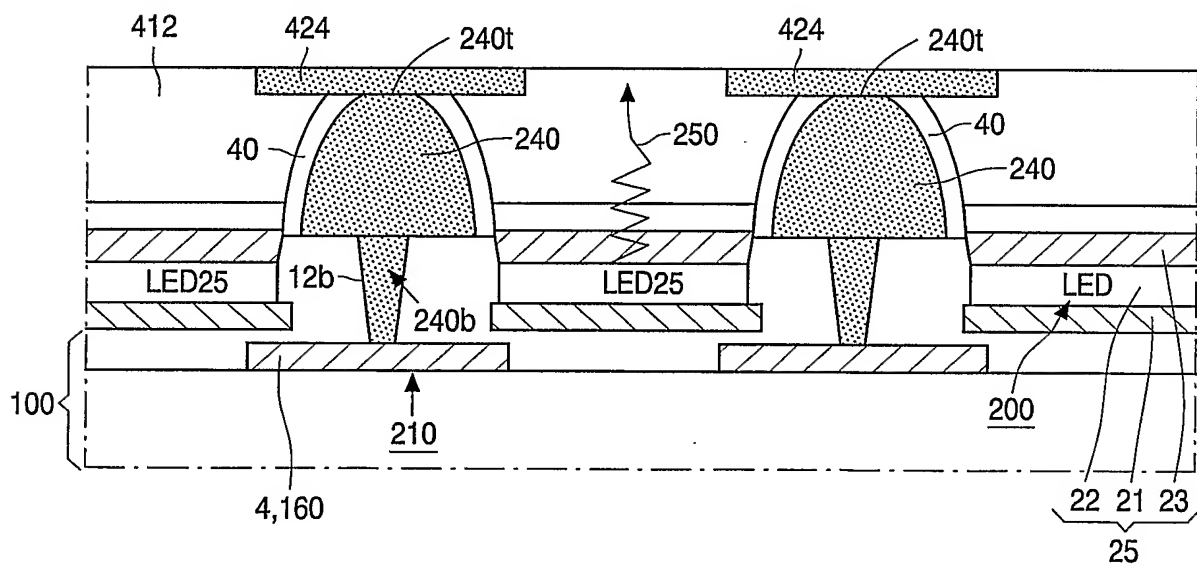


FIG. 7

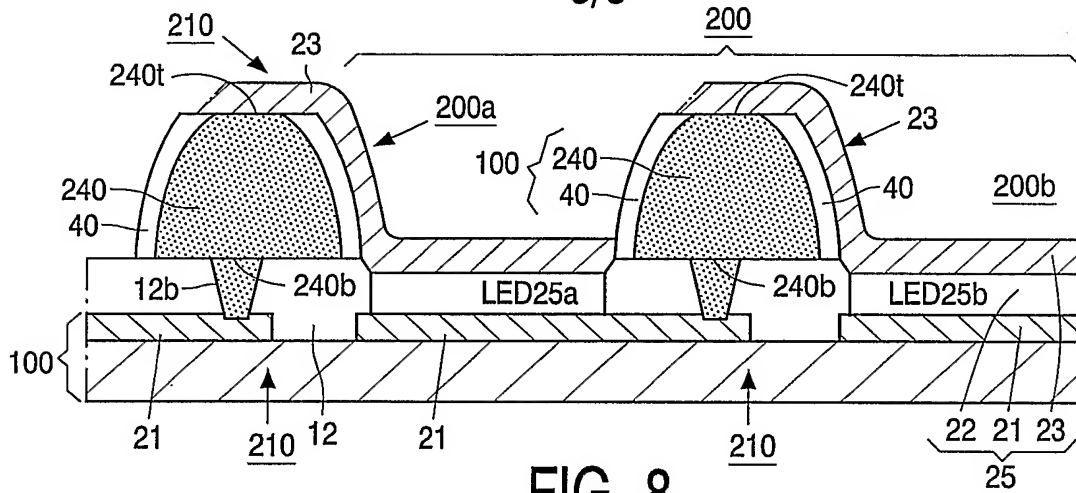


FIG. 8

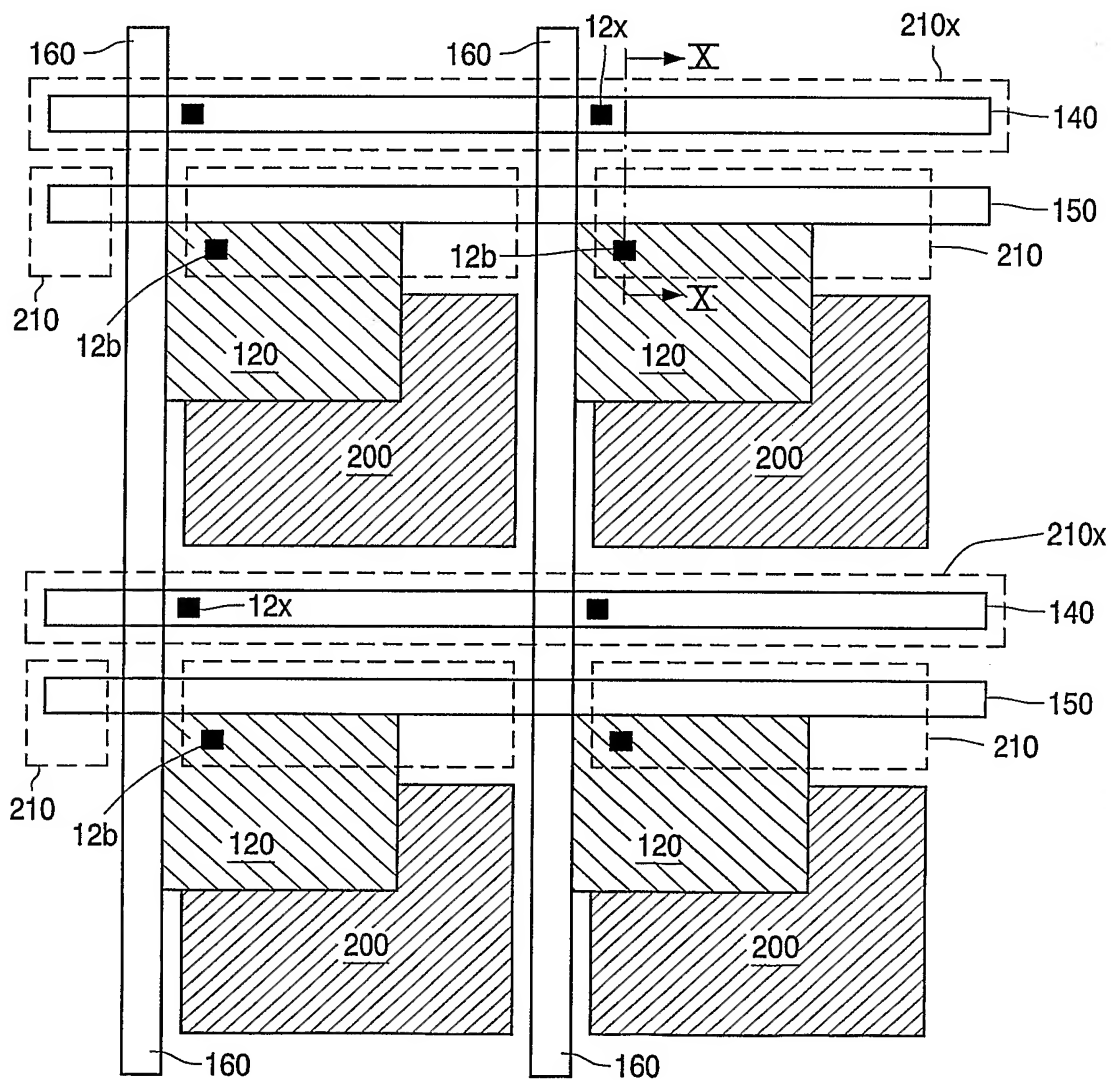


FIG. 9

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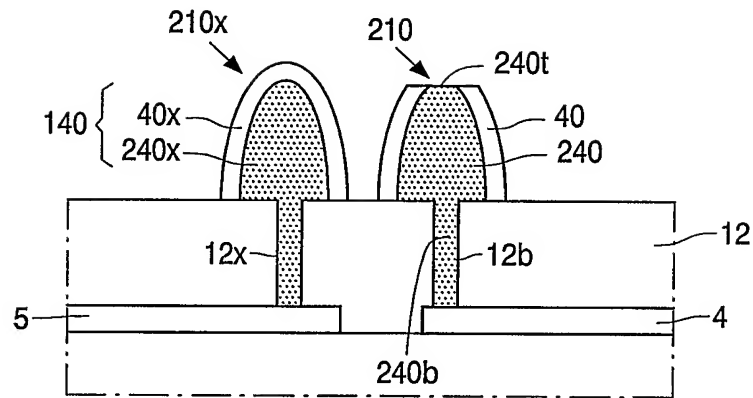


FIG. 10

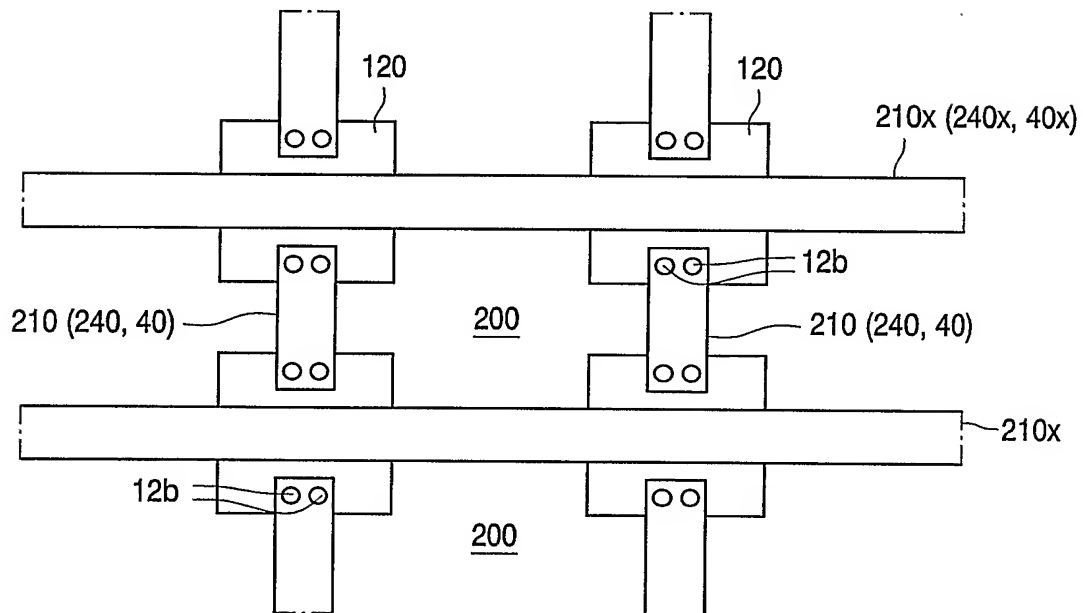


FIG. 11

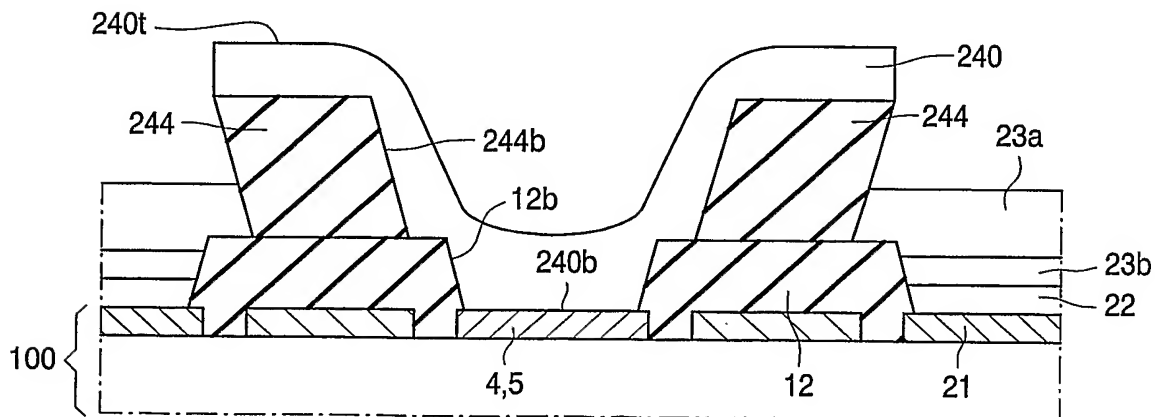


FIG. 12

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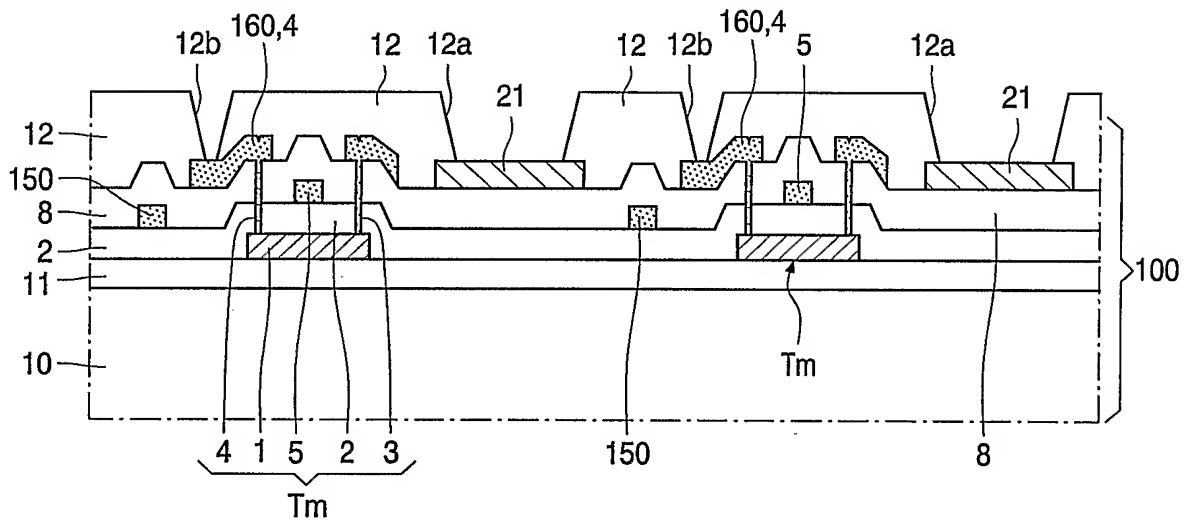


FIG. 13

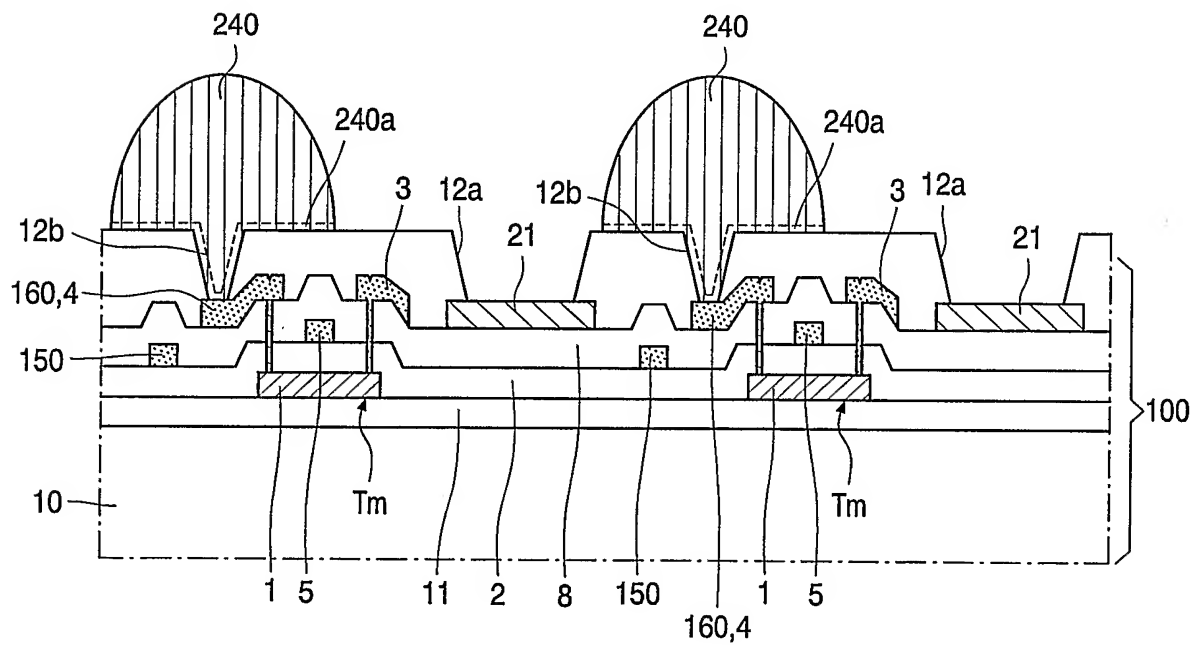


FIG. 14

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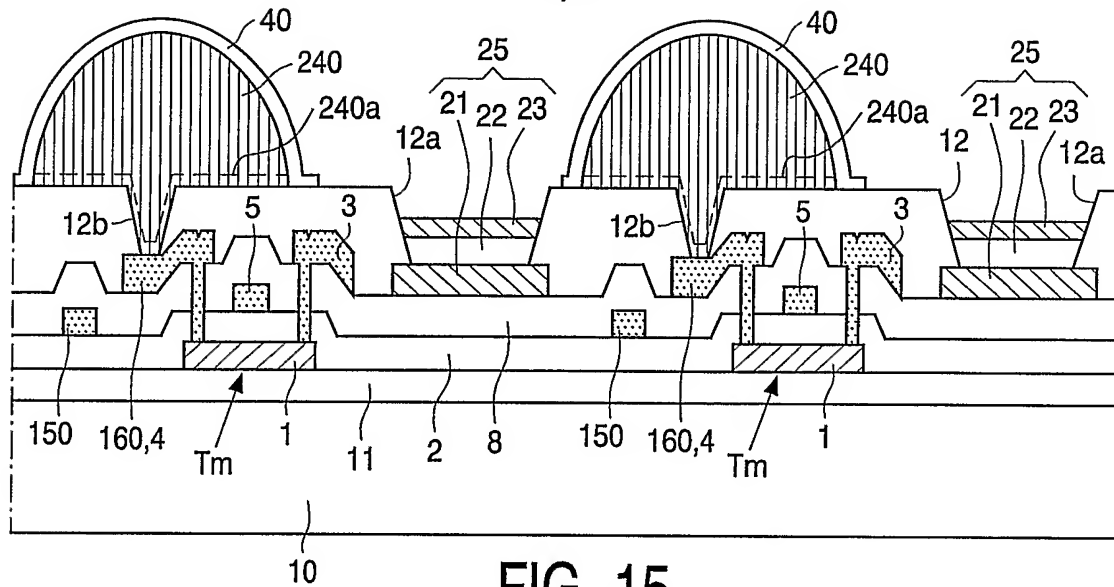


FIG. 15

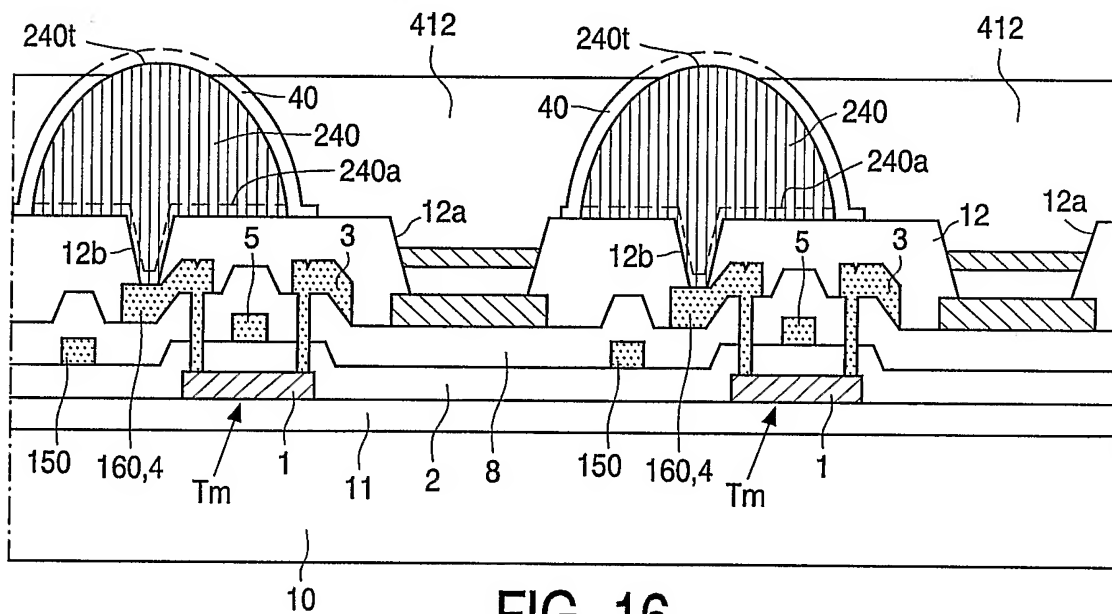


FIG. 16

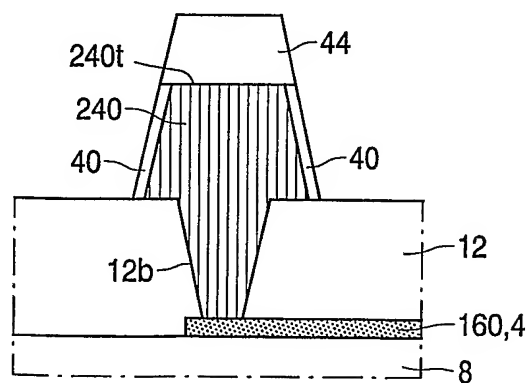


FIG. 17

## INTERNATIONAL SEARCH REPORT

International Application No

PCT/ 03/01000

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L27/15 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category <sup>a</sup>	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 307 528 B1 (YAP DANIEL) 23 October 2001 (2001-10-23) column 5, line 46 - line 51 abstract	1-19
A	--- EP 1 096 568 A (SONY CORP) 2 May 2001 (2001-05-02) abstract; figure 1	1-19
A	--- WO 01 39272 A (DEURZEN MARIA H W A VAN ; LIEDENBAUM COEN T H F (NL); DUINEVELD PAU) 31 May 2001 (2001-05-31) abstract; figure 2	1-19
A	--- EP 1 102 317 A (SONY CORP) 23 May 2001 (2001-05-23) abstract; figure 1 -----	1-19

☐ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.<sup>a</sup> Special categories of cited documents:

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Date of the actual completion of the international search

2 July 2003

Date of mailing of the international search report

17 JUL 2003

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## INTERNATIONAL SEARCH REPORT

International Application No

PCT, B 03/01000

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6307528	B1	23-10-2001	NONE	
-----				
EP 1096568	A	02-05-2001	EP 1096568 A2	02-05-2001
			JP 2001195008 A	19-07-2001
			TW 471237 B	01-01-2002
-----				
WO 0139272	A	31-05-2001	CN 1353866 T	12-06-2002
			CN 1345469 T	17-04-2002
			WO 0139272 A1	31-05-2001
			WO 0141229 A1	07-06-2001
			EP 1153445 A1	14-11-2001
			EP 1153436 A1	14-11-2001
			JP 2003515909 T	07-05-2003
			TW 478187 B	01-03-2002
-----				
EP 1102317	A	23-05-2001	JP 2001148291 A	29-05-2001
			EP 1102317 A2	23-05-2001
-----				